THE INVENTION CLAIMED IS:

1. A method for facilitating semiconductor wafer lot disposition, comprising:

providing detailed descriptive information of the semiconductor wafer layout;

generating data concerning at least one defect in the semiconductor wafers at an intermediate processing stage;

generating at least one layer model from the information and data to disclose the effects of the defect upon at least one later layer of the semiconductor wafers; and

utilizing the layer model to determine the subsequent disposition of the wafer lot.

2. The method of claim 1 wherein generating at least one layer model further comprises disclosing the components that will be located above the defect in the semiconductor wafers.

3. The method of claim 1 wherein utilizing the layer model to determine the subsequent disposition of the wafer lot further comprises treating the data concerning the defect as a new layer of information.

4. The method of claim 1 wherein utilizing the layer model to determine the subsequent disposition of the wafer lot further comprises determining whether the defect would be likely to cause at least one of: bridging at a subsequent layer, an open circuit, blockage at a later layer, and blockage between layers.

5. The method of claim 1 wherein providing detailed descriptive information of the semiconductor wafer layout further comprises providing an electronic description of the wafer layout for substantially every layer in the semiconductor wafers' fabrication process.

6. A method for facilitating semiconductor wafer lot disposition, comprising:

providing detailed descriptive information of the semiconductor wafer layout;

generating and extracting data concerning defects in the semiconductor wafers at an intermediate processing stage;

generating at least one layer model from the information and data to disclose the future effects of the current defects upon later layers at subsequent stages of the semiconductor wafers' fabrication process; and

utilizing the layer model to determine the subsequent disposition of the wafer lot.

7. The method of claim 6 wherein generating at least one layer model further comprises disclosing the components that will be located above the defects in the semiconductor wafers.

8. The method of claim 6 wherein utilizing the layer model to determine the subsequent disposition of the wafer lot further comprises treating the data concerning the defects as a new layer of information.

9. The method of claim 6 wherein utilizing the layer model to determine the subsequent disposition of the wafer lot further comprises determining whether the defects would be likely to cause at least one of: bridging at a subsequent layer, an open circuit, blockage at a later layer, and blockage between various layers.

10. The method of claim 6 wherein providing detailed descriptive information of the semiconductor wafer layout further comprises providing an electronic description of the wafer layout for substantially every layer in the semiconductor wafers' fabrication process.

11. A system for facilitating semiconductor wafer lot disposition, comprising:

means for providing detailed descriptive information of the semiconductor wafer layout;

means for generating data concerning at least one defect in the semiconductor wafers at an intermediate processing stage;

means for generating at least one layer model from the information and data to disclose the effects of the defect upon at least one later layer of the semiconductor wafers; and

means for utilizing the layer model to determine the subsequent disposition of the wafer lot.

12. The system of claim 11 wherein the means for generating at least one layer model further comprises means for disclosing the components that will be located above the defect in the semiconductor wafers.

13. The system of claim 11 wherein the means for utilizing the layer model to determine the subsequent disposition of the wafer lot further comprises means for treating the data concerning the defect as a new layer of information.

14. The system of claim 11 wherein the means for utilizing the layer model to determine the subsequent disposition of the wafer lot further comprises means for determining whether the defect would be likely to cause at least one of: bridging at a subsequent layer, an open circuit, blockage at a later layer, and blockage between layers.

15. The system of claim 11 wherein the means for providing detailed descriptive information of the semiconductor wafer layout further comprises means for providing an electronic description of the wafer layout for substantially every layer in the semiconductor wafers' fabrication process.

16. A system for facilitating semiconductor wafer lot disposition, comprising:

means for providing detailed descriptive information of the semiconductor wafer layout;

means for generating and extracting data concerning defects in the semiconductor wafers at an intermediate processing stage;

means for generating at least one layer model from the information and data to disclose the future effects of the current defects upon later layers at subsequent stages of the semiconductor wafers' fabrication process; and

means for utilizing the layer model to determine the subsequent disposition of the wafer lot.

17. The system of claim 16 wherein the means for generating at least one layer model further comprises means for disclosing the components that will be located above the defects in the semiconductor wafers.

18. The system of claim 16 wherein the means for utilizing the layer model to determine the subsequent disposition of the wafer lot further comprises means for treating the data concerning the defects as a new layer of information.

19. The system of claim 16 wherein the means for utilizing the layer model to determine the subsequent disposition of the wafer lot further comprises means for determining whether the defects would be likely to cause at least one of: bridging at a subsequent layer, an open circuit, blockage at a later layer, and blockage between various layers.

20. The system of claim 16 wherein the means for providing detailed descriptive information of the semiconductor wafer layout further comprises means for providing an electronic description of the wafer layout for substantially every layer in the semiconductor wafers' fabrication process.